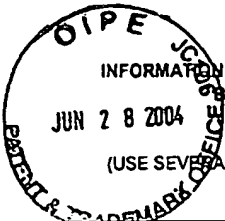


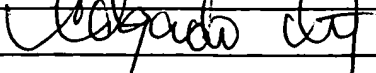
FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE  INFORMATION DISCLOSURE STATEMENT BY APPLICANT (USE SEVERAL SHEETS IF NECESSARY)	ATTY. DOCKET NO. ZLINK.026A	APPLICATION NO. 10/826,891
	APPLICANT LeReverend, Remi	
	FILING DATE April 16, 2004	GROUP Unknown 2815

U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
EO	1.	6,097,242	8/1/00	Forbes et al.			
EO	2.	U.S. Patent Publication No.: 2002/0093382 A1	July 18, 2002	Gupta			

FOREIGN PATENT DOCUMENTS									
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION		
							YES	NO	

EXAMINER INITIAL	OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)							
EO	3.	Eric A. Vittoz, <i>Micropower Techniques</i> , Design of VLSI Circuits for Telecommunications and Signal Processing, pp. 53-97 (J.E. Franca and Y.P. Tsividis eds., Prentice Hall, 1994)						
EO	4.	Namkyu Park, et al., <i>Body Bias Dependence of 1/f Noise in NMOS Transistors From Deep-Subthreshold to Strong Inversion</i> , IEEE Transactions on Electron Devices, Vol. 48, No. 5, pp. 999-1001 (May 2001)						
EO	5.	Clement Wann, et al., <i>CMOS With Active Well Bias for Low-Power and RF/Analog Applications</i> , IEEE - 2000 Symposium on VLSI Technology Digest of Technical Papers, pp. 158-159						
EO	6.	Ming-Jer Chen, et al., <i>Dependence of Current Match on Back-Gate Bias in Weakly Inverted MOS Transistors and its Modeling</i> , IEEE Journal of Solid-State Circuits, Volume 31, No. 2, pp. 259-262 (February 1996)						
EO	7.	Shih-Fen Huang, et al., <i>Scalability and Biasing Strategy for CMOS with Active Well Bias</i> , 2001 Symposium on VLSI Technology Digest of Technical Papers, pp. 107-108						
EO	8.	Rajesh H. Zele, <i>Low-Power CMOS Continuous-Time-Filters</i> , IEEE Journal on Solid-State Circuits, Volume 31, No. 2, pp. 157-168 (February 1996)						

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EXAMINER		DATE CONSIDERED	9/27/05
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